IN THE SPECIFICATION:

Please replace paragraph [0047] with the following paragraph:

Metal layer 650 is deposited overlying thin oxide layer 580, field oxide layer 590, PSG layer 600, polysilicon layer 610, epitaxial layer 520, and semiconductor substrate 510. Metal layer 650 is subsequently patterned to form interconnect of the high voltage power transistor including the contact regions of the first, control, and second electrodes of the power transistor. The metal contact regions further include areas for receiving solder bumps. Metal layer 650 also resides on the side walls and bottom area of deep trench 640. Thus, the metal contact region of the first electrode extends into deep trench 640 directly contacting semiconductor substrate 510. Metal layer ~~560~~ 650 couples to polysilicon layer 610 through opening 550 corresponding to the control electrode and epitaxial layer 520 through opening 540 corresponding to the second electrode of the high voltage power transistor.